ABSTRACT OF THE DISCLOSURE

Selfaligned Source/Drain FinFET Process Flow

A selfaligned FinFET is fabricated by defining a set of fins in a semiconductor wafer, depositing gate material over the fins, defining a gate hardmask having a thickness sufficient to withstand later etching steps, etching the gate material outside the hardmask to form the gate, depositing a conformal layer of insulator over the gate and the fins, etching the insulator anistotropically until the insulator over the fins is removed down to the substrate, the hardmask having a thickness such that a portion of the hardmask remains over the gate and sidewalls remain on the gate, and forming source and drain areas in the exposed fins while the gate is protected by the hardmask material.